

Appl. No. 10/708,128  
Amdt. dated November 25, 2005  
Reply to Office action of August 26, 2005

**Amendments to the Claims:**

1. (Currently amended) A method of forming a transistor on a semiconductor substrate comprising:
- forming at least one gate structure on the semiconductor substrate;
- 5 performing a surface cleaning process, the surface cleaning process comprising:
- utilizing a chemical oxidation method for forming a first oxide layer on a surface of the semiconductor substrate ~~not covered with and~~ a second oxide layer on a surface of the gate structure; and
- removing the first oxide layer and the second oxide layer simultaneously; and
- 10 utilizing a selective epitaxial growth method for forming a first epitaxial layer on the surface of the semiconductor substrate.
2. (Original) The method of claim 1 further comprising performing the surface cleaning process repeatedly for removing a first thickness of the semiconductor substrate.
- 15 3. (Original) The method of claim 2 wherein the chemical oxidation method utilizes an oxidant acid to form the first oxide layer.
4. (Original) The method of claim 3 wherein the surface cleaning process utilizes a
- 20 diluted hydrofluoric acid to remove the first oxide layer.
5. (Original) The method of claim 4 wherein the oxidant acid is a mixture comprising sulfuric acid (H<sub>2</sub>SO<sub>4</sub>), hydrogen peroxide (H<sub>2</sub>O<sub>2</sub>), and deionized water.
- 25 6. (Original) The method of claim 5 wherein a volume ratio of sulfuric acid to hydrogen peroxide is approximately 4 to 1, and a temperature of the oxidant acid is about 125°C.
7. (Original) The method of claim 4 wherein the oxidant acid is a mixture comprising

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sulfuric acid ( $\text{H}_2\text{SO}_4$ ), ozone ( $\text{O}_3$ ), and deionized water, and a temperature of the oxidant acid is about  $35^\circ\text{C}$ .

8. (Original) The method of claim 2 wherein a thickness of the first oxide layer  
5 approximately ranges from 15 angstroms ( $\text{\AA}$ ) to 30 angstroms, and the first thickness approximately ranges from 10 angstroms to 50 angstroms.

9. (Original) The method of claim 2 wherein forming the gate structure comprises the following steps:  
10 forming a gate oxide layer on a portion of the semiconductor substrate;  
forming a gate electrode on the gate oxide layer;  
forming a liner oxide layer on the semiconductor substrate to cover the gate electrode;  
forming a dielectric layer on the liner oxide layer; and  
15 performing an etching-back process on the liner oxide layer and the dielectric layer to form a spacer on sidewalls of the gate electrode;  
wherein the gate structure comprises the gate oxide layer, the gate electrode, and the spacer.

20 10. (Cancelled)

11. (Cancelled)

12. (Currently amended) The method of claim ~~4~~ 1 wherein the selective epitaxial growth  
25 method further comprises forming a second epitaxial layer on the surface of the gate electrode.

13. (Original) The method of claim 9 further comprising performing an ion-implantation

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process for forming a source electrode in the semiconductor substrate adjacent to one side of the gate structure and forming a drain electrode in the semiconductor substrate adjacent to another side of the gate structure.

5 14. (Original) The method of claim 13 wherein the ion-implantation process is performed before the surface cleaning process is performed.

15. (Original) The method of claim 13 wherein the ion-implantation process is performed after the first epitaxial layer is formed.

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16. (Original) The method of claim 12 further comprising forming silicide layers on both the first epitaxial layer and the second epitaxial layer.

15 17. (Original) The method of claim 12 wherein the semiconductor substrate is a silicon substrate, and the first epitaxial layer and the second epitaxial layer are both silicon epitaxial layers.

18. (Cancelled)

20 19. (Cancelled)

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23. (Cancelled)

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24. (Cancelled)

25. (Cancelled)

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26. (Cancelled)